REMARKS

Claims 1-4, 7-8, 11, 18-20, 23, 24, 33-36, 39-40, 43, 50-52, 55-56 and 65-66 were rejected under 35 U.S.C. 102(e) as being anticipated by Kermani et al., U.S. Patent 6,275,068. The remaining claims have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani et al. in view of Bae, U.S. Patent 6,242,960. Those rejections are respectfully traversed and reconsideration is requested.

Independent claims 1 and 33 are directed to a data transmitter which controls the transition time of a data signal, that is the time that it takes for the data signal to change from one state to the next. As illustrated in Figure 2, an input data signal din has very short transition times from low to high and from high to low. By contrast, the data signal dout has a substantially longer transition time t_r from low to high. This long transition time is obtained by applying the data signal to parallel delay circuits as illustrated, for example, in Figures 1 and 3. The data signal output from each of those delays has a transition time t_{r1} illustrated in Fig. 2. However, by summing the multiple delayed signals at a common output node, it can be seen that the combined transition time of the summed signals d1'-d4' provides the longer transition t_r of signal dout.

Neither of the cited references discloses a data transmitter and neither allows the determination of a transition time. Further, neither combines delayed data signals.

Kermani et al. describes a clock de-skew circuit that controls the relative delays of CLK0 and CLK1. The signals AD1-AD4 and EN1-EN8 are not data inputs, and no delay is applied to those signals. Rather, those signals are control signals that control the delay applied to the clock signals CLKIN0 and CLKIN1.

Kermani et al. has parallel delay circuits which delay the respective clock signals CLKIN0 and CLKIN1, not data signals. Further, those delay circuits are not combined at the respective outputs 55 and 62 and do not control the transition times of the clock signals. Rather, only one of signals EN1-EN4 is enabled and one of signals EN5-EN8 is enabled at any time, as is evident from tables 3 and 4. In looking to Figure 2 of the present application, if one were to

compare the delayed clock signals of Kermani et al. to the delayed data signals of Figure 2 of the present application, Kermani et al. would only select one of the delayed signals so there would be a single transition time t_{t1}. Since only one of the delayed signals is enabled, there is no combining of the delayed signals to provide the longer transition time t_t.

With respect to claims 18 and 50, and with reference to Figure 5, a transition time can be made proportional to bit time of the bit clock by appropriately controlling the control signal 151 as illustrated in Fig. 6. That control signal may be generated using a phase comparator and a feedback loop in a circuit having parallel delay elements. Neither of the cited references relates to control of transition time of a data signal, much less controlling such transition time to be proportional to bit time of a bit clock.

Nor does Bae satisfy the deficiencies of Kermani et al. Bae discloses a pulse generator circuit in which a clock signal passes through a pair of delay lines to generate a pulse which is in turn used to generate an output clock PCLK. The delayed clock signals are combined in combinational logic and do not determine a transition time. Nor does Bae suggest a phase comparator or control of a supply voltage to delay elements as recited in dependent claims 12-17, 27-32, 44-49 and 59-64.

CONCLUSION

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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